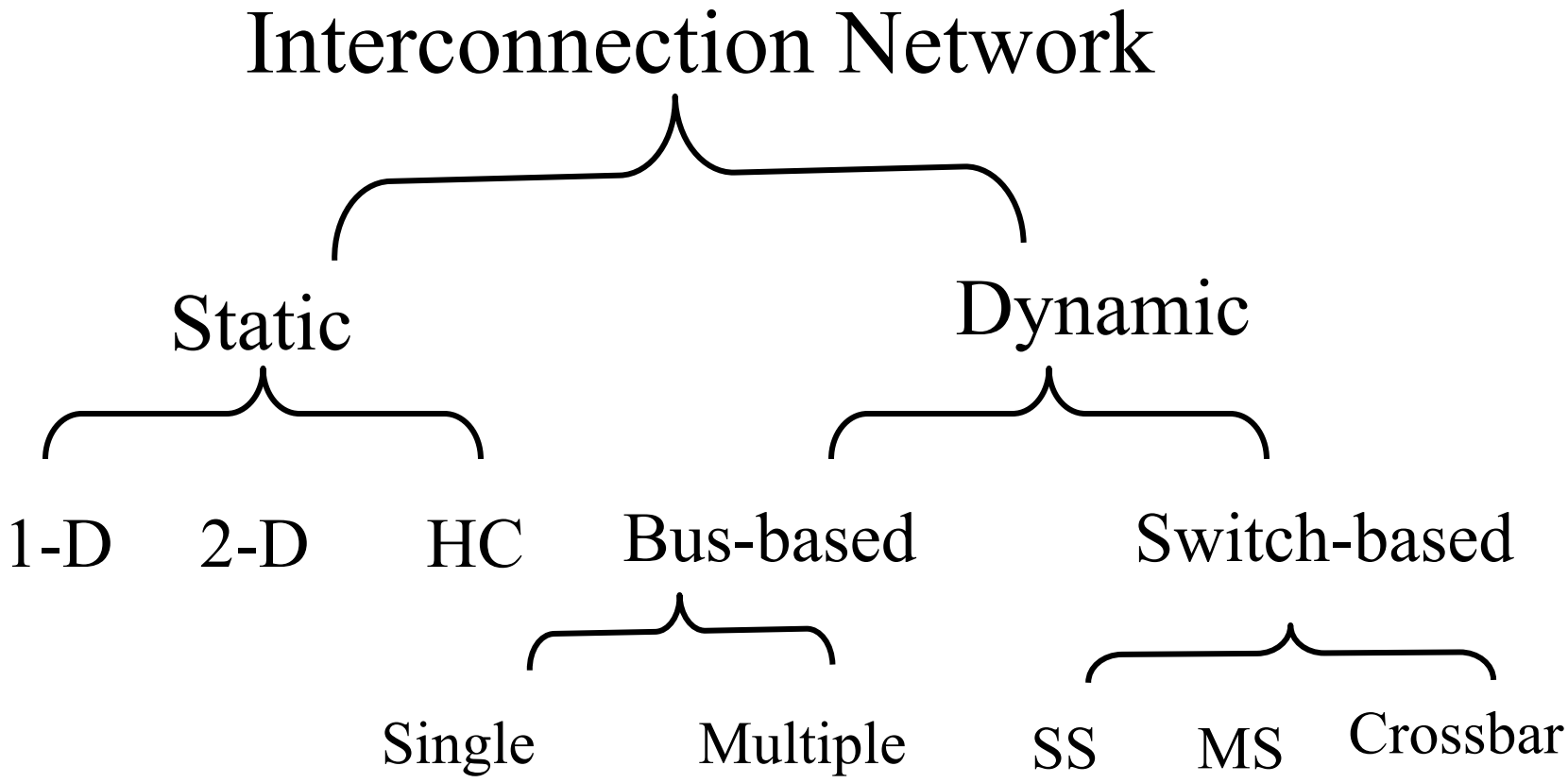
Chapter 2

Multiprocessors Interconnection Networks

2.1 Interconnection Networks Taxonomy

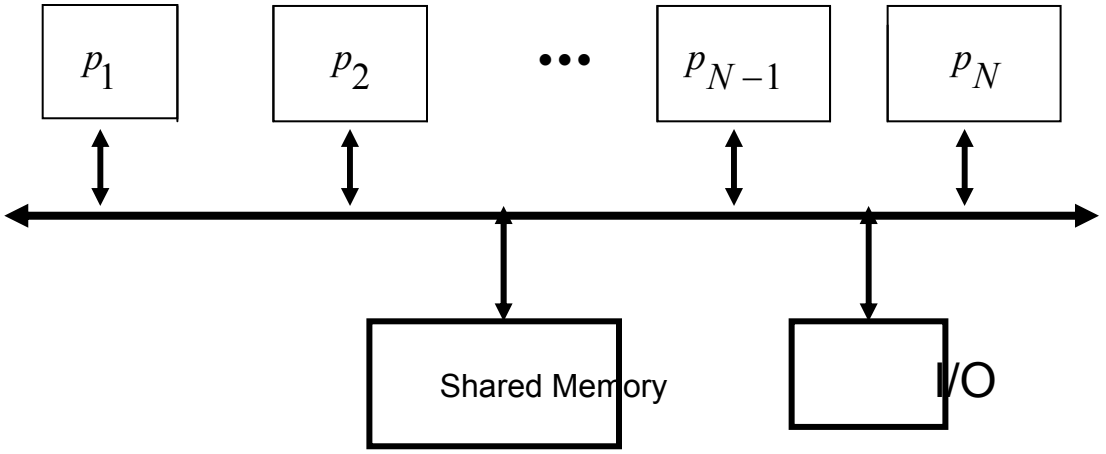


2.2 Bus-Based Dynamic Interconnection Networks

- Single Bus Systems
  - Simplest way to connect multiprocessor systems.
  - The use of local caches reduces the processor-memory traffic.
  - Size of such system varies between 2 and 50 processors.
  - Single bus multiprocessors are inherently limited by:
    - Bandwidth of bus.
    - 1 processor can access the bus.
    - 1 memory access can take place at any given time.

2.2 Bus-Based Dynamic Interconnection Networks

- Single Bus Systems



2.2 Bus-Based Dynamic Interconnection Networks

- Multiple Bus Systems
  - Several parallel buses to interconnect multiple processors and multiple memory modules.
  - Many connection schemes are possible.
  - Examples:
    - Multiple Bus with Full Bus – Memory Connection (MBFBMC).
    - Multiple Bus with Single Bus – Memory Connection (MBSBMC).
    - Multiple Bus with Partial Bus – Memory Connection (MBPBMC).
    - Multiple Bus with Class-based Bus – Memory Connection (MBCBMC).

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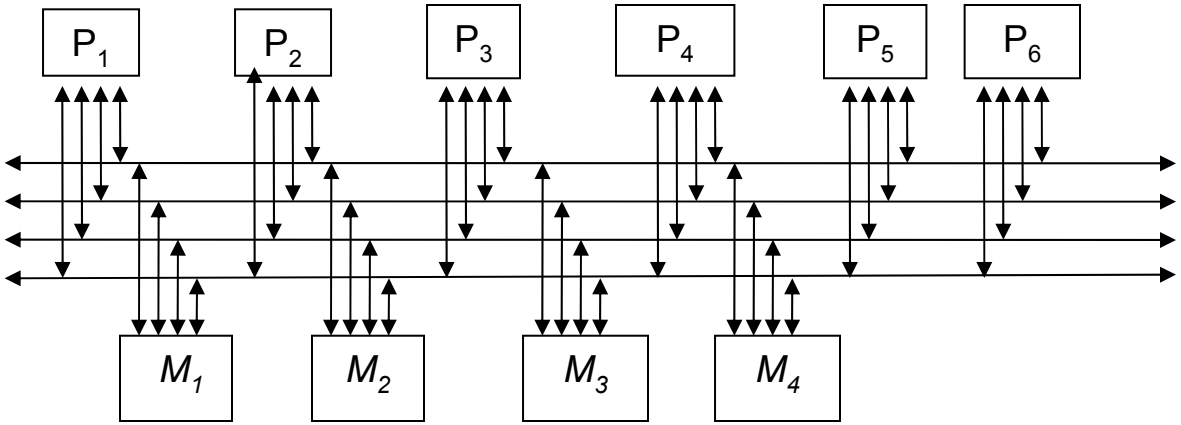

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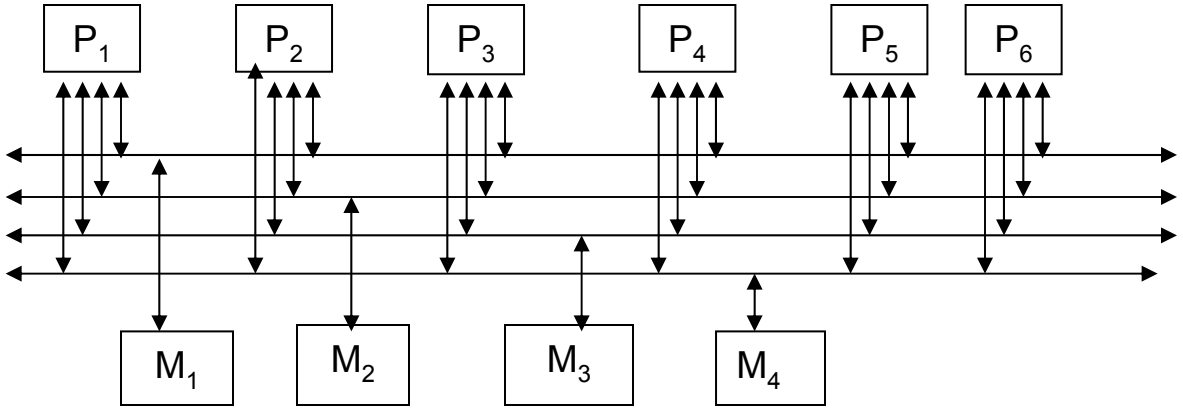

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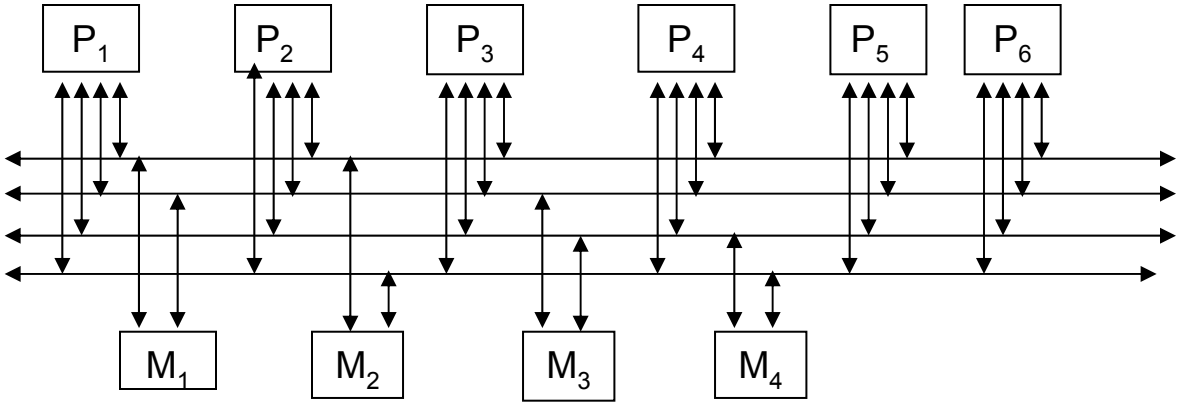

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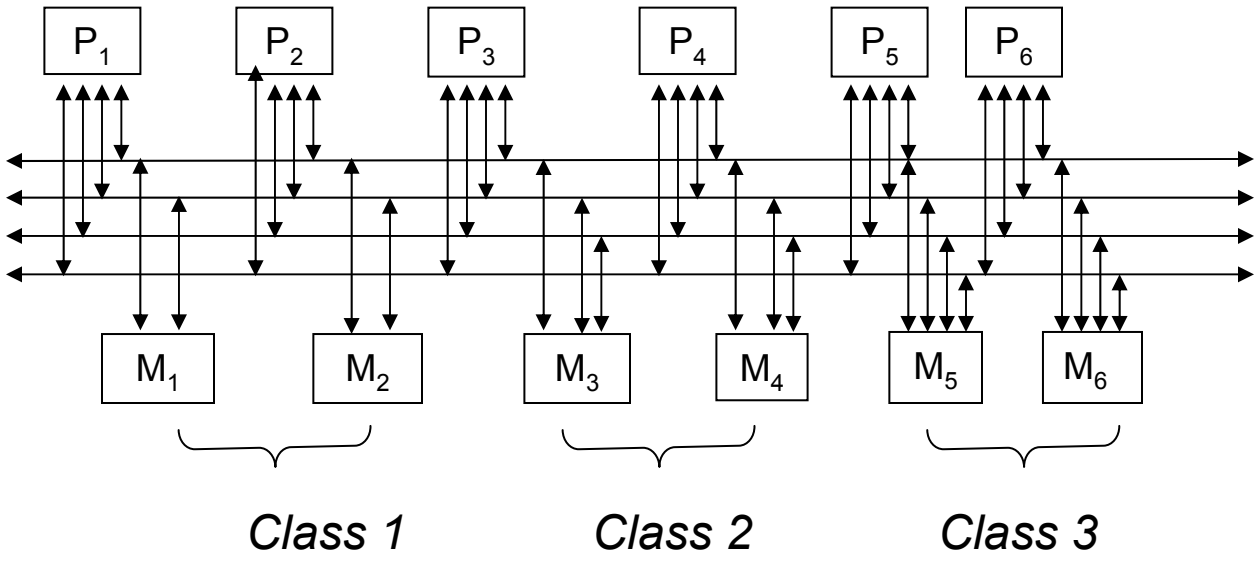


2.2 Bus-Based Dynamic Interconnection Networks

- Bus Synchronization
  - A bus can be synchronous:
    - Time for any transaction is known in advance.
  - A bus can be asynchronous:
    - Depends on the availability of data and readiness of devices to initiate bus transactions.
  - Bus arbitration logic is required to resolve bus contention when more than 1 processor compete to access the bus in single bus multiprocessor.
    - Process of passing mastership from 1 processor to another is called handshaking
      - Requires a bus request and a bus grant.

2.2 Bus-Based Dynamic Interconnection Networks

- Bus Synchronization
  - Bus arbitration logic uses a a predefined priority scheme:
    - Random
    - Simple rotating
    - Equal priority
    - Least Recently Used (LRU)

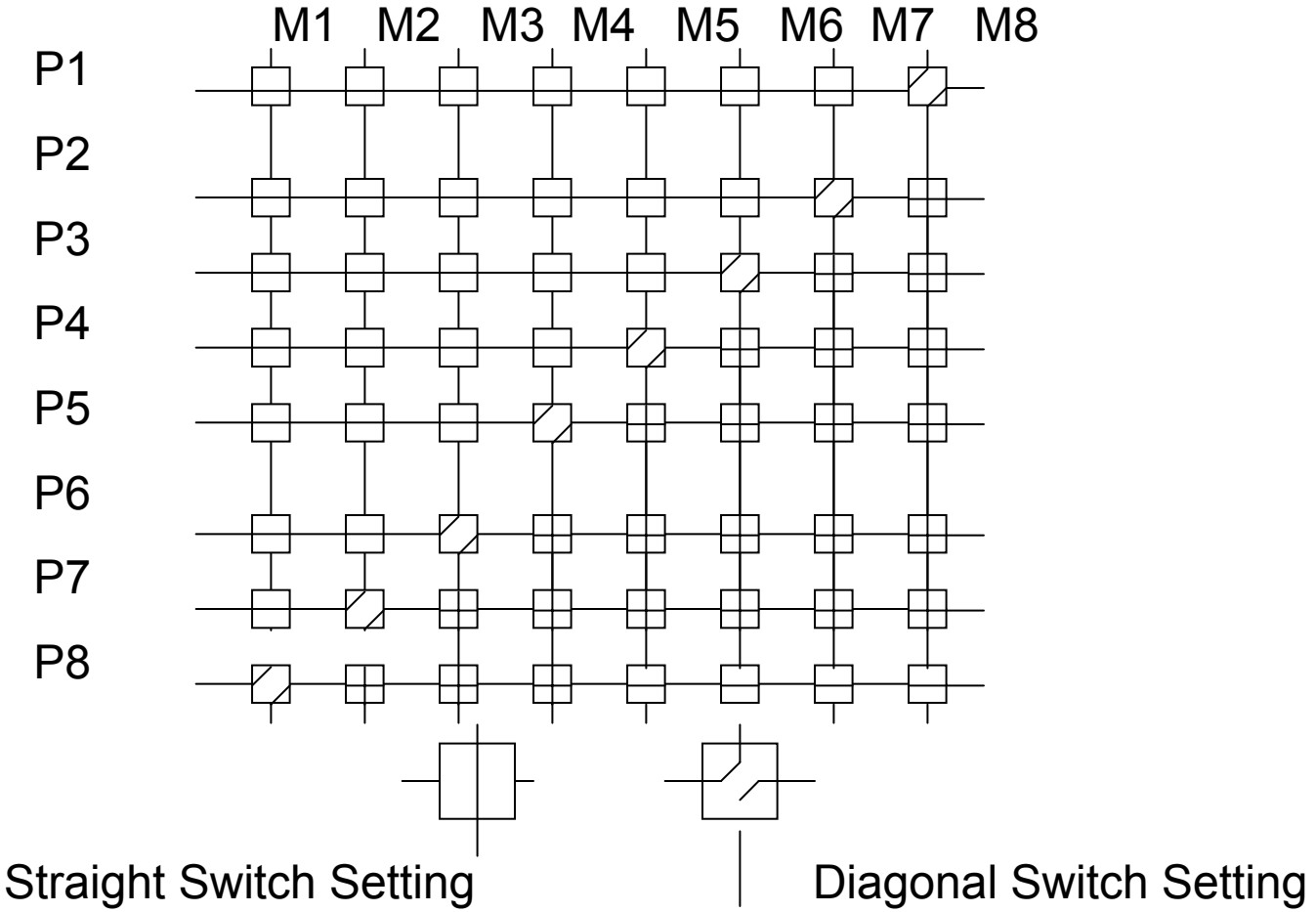
2.3 Switch-Based Interconnection Networks

– Crossbar Networks

- Provide simultaneous connections among all its inputs and all its outputs.
- A Switching Element (SE) is at the intersection of any 2 lines extended horizontally or vertically inside the switch.
- It is a non-blocking network allowing multiple input-output connection pattern to be achieved simultaneously.

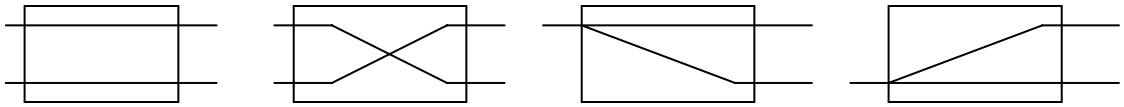
2.3 Switch-Based Interconnection Networks

– Crossbar Networks



2.3 Switch-Based Interconnection Networks

- Single-Stage Networks
  - A single stage of SE exists between the inputs and outputs of the network.
  - Possible settings of a 2x2 SE are:



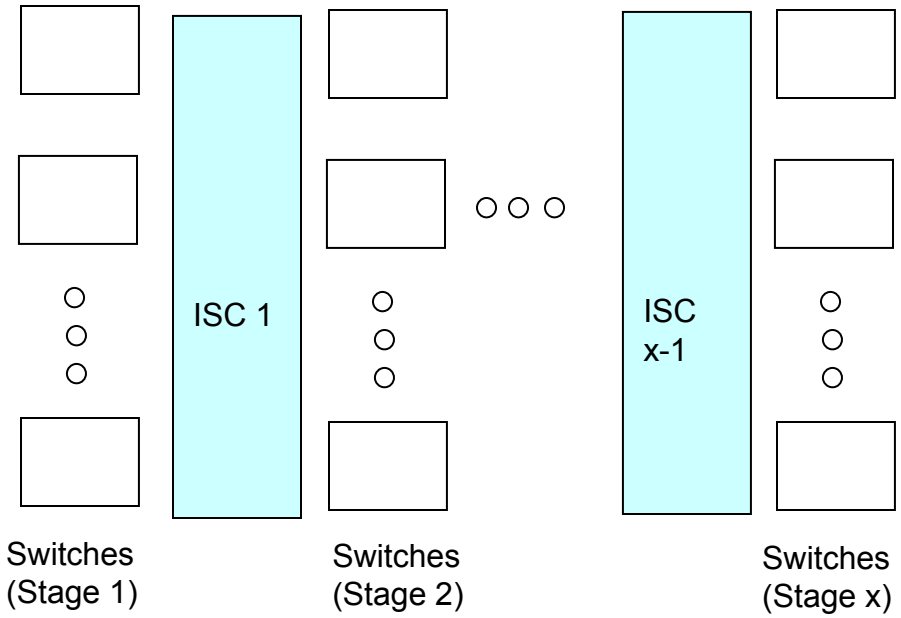
Straight Exchange Upper-broadcast Lower-broadcast

2.3 Switch-Based Interconnection Networks

- Multistage Interconnection Networks (MINs)
  - A MIN consists of a number of stages each consisting of a set of 2x2 SEs.
  - Stages are connected to each other using Inter-Stage Connection (ISC) pattern.
  - In MINs the routing of a message from a given source to a given destination is based on the destination address (self-routing).

2.3 Switch-Based Interconnection Networks

- Multistage Networks (MINs)



2.3 Switch-Based Interconnection Networks

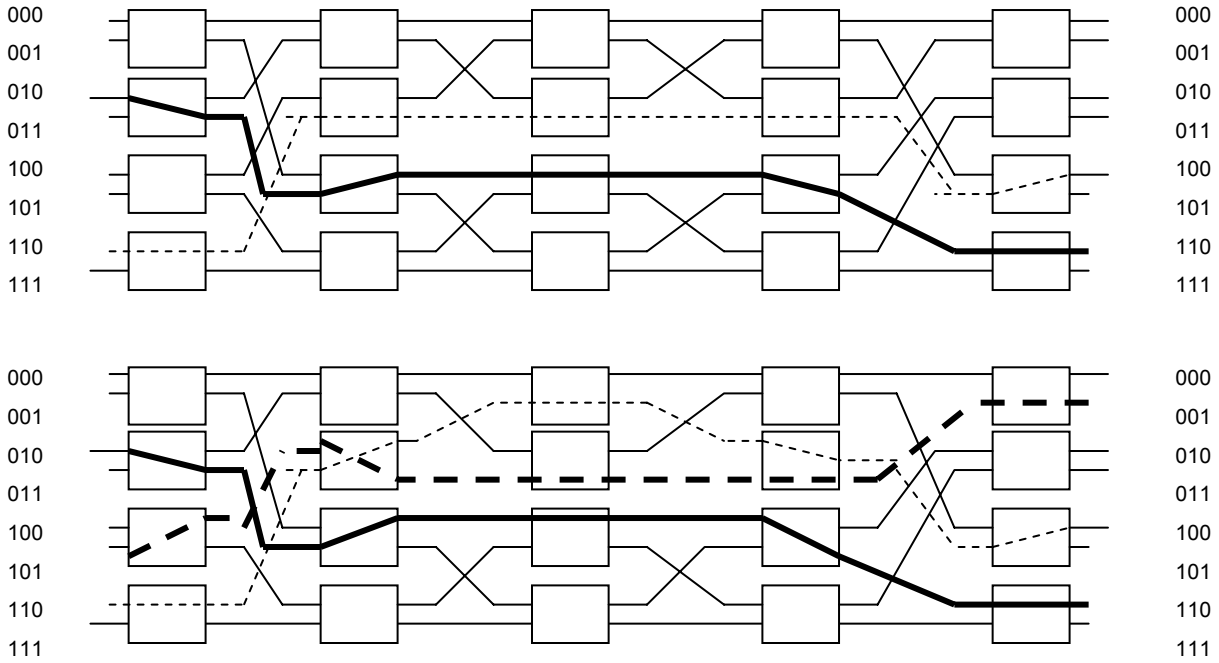
- Blockage in Multistage Interconnection Networks
  - Blocking networks:
    - when an interconnection between a pair of input/output is currently established, the arrival of a request for a new interconnection between 2 arbitrary unused input and output may or may not be possible.

2.3 Switch-Based Interconnection Networks

- Blockage in Multistage Interconnection Networks
  - Rearrangeable networks:
    - Always possible to rearrange already established connections in order to make allowance for other connections to be established simultaneously

2.3 Switch-Based Interconnection Networks

- Blockage in Multistage Interconnection Networks
  - Rearrangeable networks



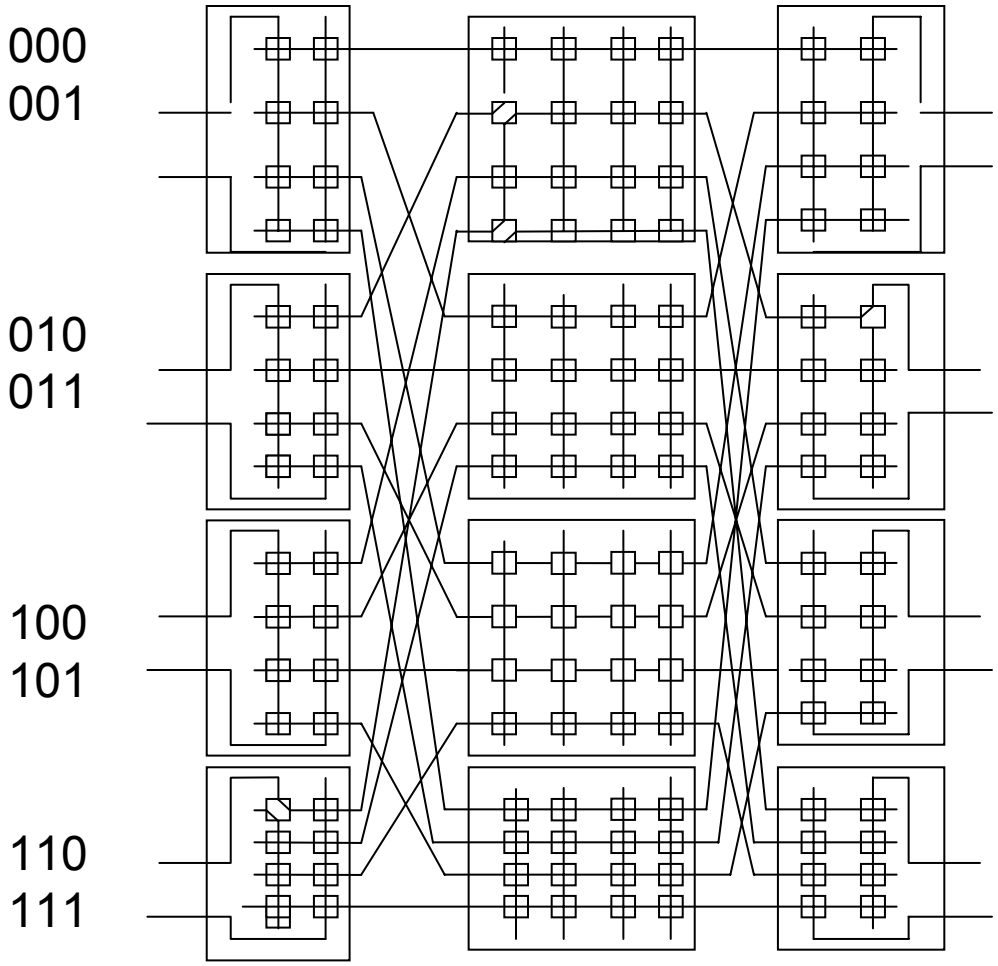
2.3 Switch-Based Interconnection Networks

- Blockage in Multistage Interconnection Networks
  - Non-blocking networks:
    - In presence of a currently established connection between any pair of input/output, it is always possible to establish a connection between any arbitrary unused pair of input/output.

2.3 Switch-Based Interconnection Networks

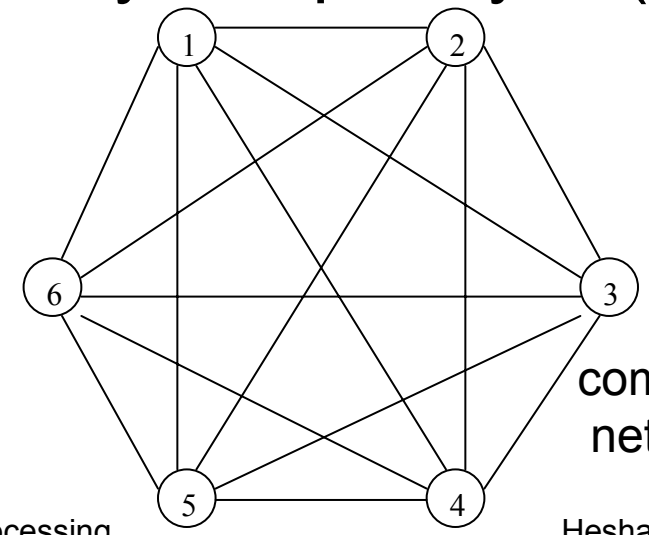
- Blockage in Multistage Interconnection Networks
  - Non-blocking networks:

2.3 Switch-Based Interconnection Networks



2.4 Static Interconnection Networks

- Have fixed paths, unidirectional or bi-directional, between processors.
- Types:
  - Completely connected networks: Number of links: $O(N^2)$, delay complexity: O(1).

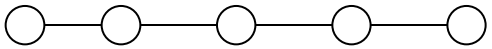


completely connected network.

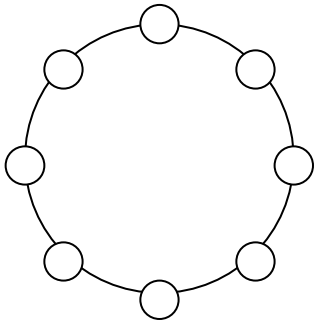
2.4 Static Interconnection Networks

- Limited Connection Networks:
  - Linear arrays
  - Ring (Loop) networks
  - Two-dimensional arrays
  - Tree networks
  - Cube network

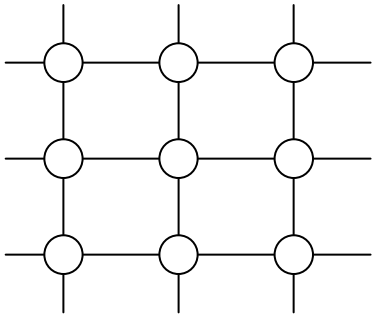
2.4 Static Interconnection Networks



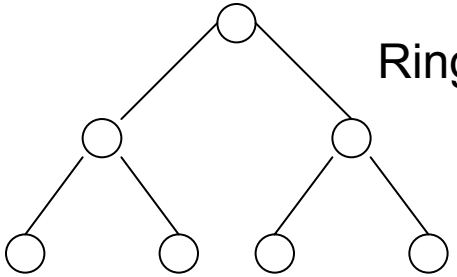
Linear arrays



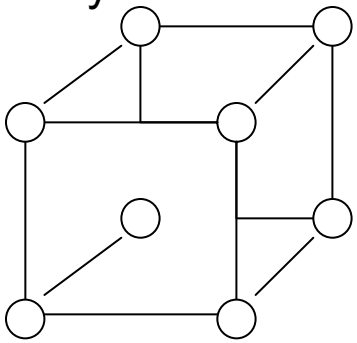
Ring (Loop) networks



Two-dimensional arrays



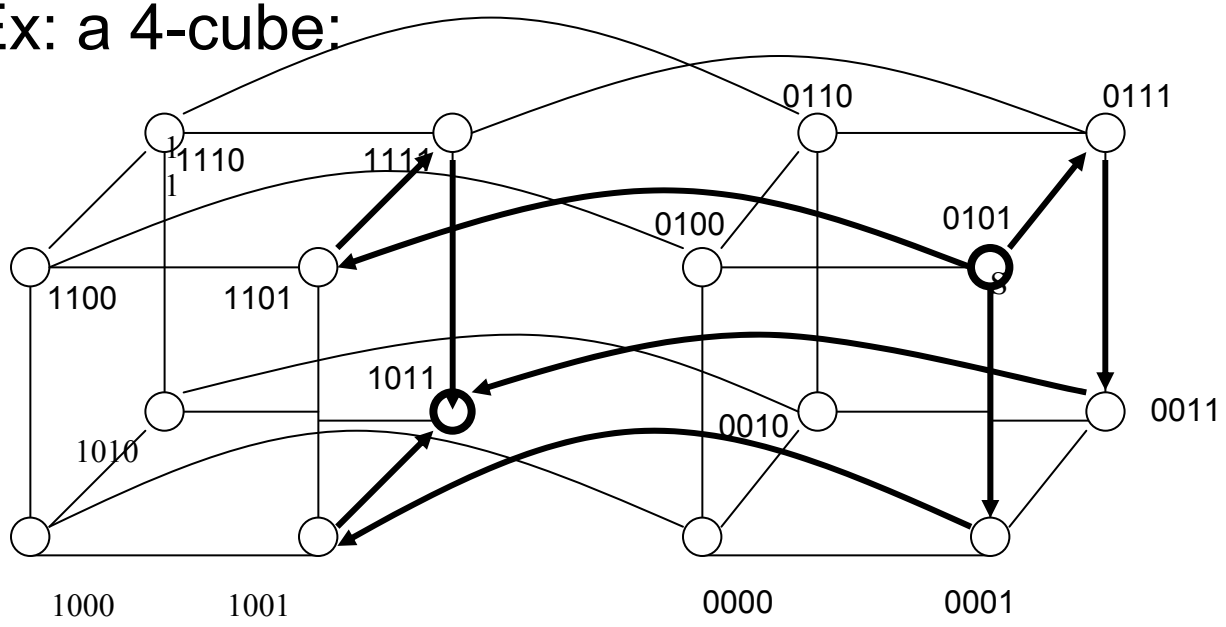
Tree networks



Cube network

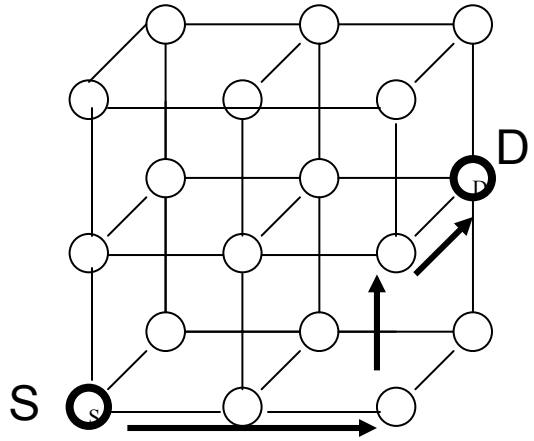
2.4 Static Interconnection Networks

– Cube Connected Networks:
  - Patterned after the n-cube structure
  - In an n-cube, every processor is connected to n others
  - Ex: a 4-cube:



2.4 Static Interconnection Networks

– Mesh Connected Networks:



Example 3X3X2 mesh network

2.5 Analysis and Performance Metrics

- Dynamic Networks

Networks	Delay	Cost	Blocking	Degree of FT
Bus	O(N)	O(1)	Yes	0
Multiple-bus	O(mN)	O(m)	Yes	(m-1)
MIN	O(logN)	O(NlogN)	Yes	0
Crossbar	O(1)	$O(N^2)$	No	0

2.5 Analysis and Performance Metrics

- Static Networks

Networks	Degree (d)	Diameter (D)	Cost (No. of links)	Symmetry	Worst Delay
CCNs	N-1	1	N(N-1)/2	Yes	1
Linear array	2	N -1	N -1	No	N
Binary tree	3	$2(\lceil \mathrm{Log}_2 N \rceil - 1)$	N -1	No	Log_2 N
n-cube	Log_2 N	Log_2 N	nN/2	Yes	Log_2 N
2D-mesh	4	2(n-1)	2(N-n)	No	$\sqrt{N}$
K-ary n-cube	2n	$N/\lceil k/2 \rceil$	n x N	Yes	k x $\log_2$ N

2.6 Summary

- Different topologies used for interconnecting multiprocessors were discussed.
- Taxonomy for interconnection networks based on their topology is introduced.
- Dynamic and static interconnection schemes have been studied.
- A number of basic performance aspects related to both dynamic and static interconnection networks have been introduced.